CLAIMS

1) A circuit (IC) comprising a microprocessor (MIC) and a set of peripheral devices comprising at least one communication interface (UMI) for external access, wherein said peripherals (PER), unlike the said communication interface (UMI), are connected to the said microprocessor MIC by an interconnection bus (BUS),

characterised in that it also comprises a security module (CR) connected to the said interconnection bus BUS and to the said communication interface (UMI) by a dedicated link (DL).

2) A circuit according to claim 1, characterised in that the said communication interface (UMI) is adapted to an external memory (MEM).

3) A circuit according to claim 1 or 2, characterised in that the said security module comprises encryption means (CR).

4) A circuit according to claim 3, characterised in that the said encryption means (CR) use a private key.

5) A circuit according to claim 3 or 4, characterised in that, since the encryption key is longer than the standard length of the data processed by the said microprocessor (MIC), it comprises means for breaking the said encrypted words down into standard-length data.

6) A circuit according to claim 4, characterised in that, since it also comprises a cache memory

associated to a controller, and since the encryption key is longer than the standard length of the data processed by the said microprocessor (MIC), the said security module (CR) is able to process consecutive accesses of the said controller in order to break the said encrypted words down into standard-length data.

7) A circuit according to any of the claims 3 to 6, characterised in that the encryption key is stored in a one-time-programmable register.

8) A circuit according to claim 7, characterised in that, since it comprises a non-volatile memory, the said register is stored in this non-volatile memory.